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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,780	12/21/2000	Martin C. Roberts	303.451US6	3144

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EXAMINER
COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,780	ROBERTS ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *38-45,47-65 and 68-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *38-45,47-65 and 68-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed July 6, 2004 have been fully considered but they are not persuasive.

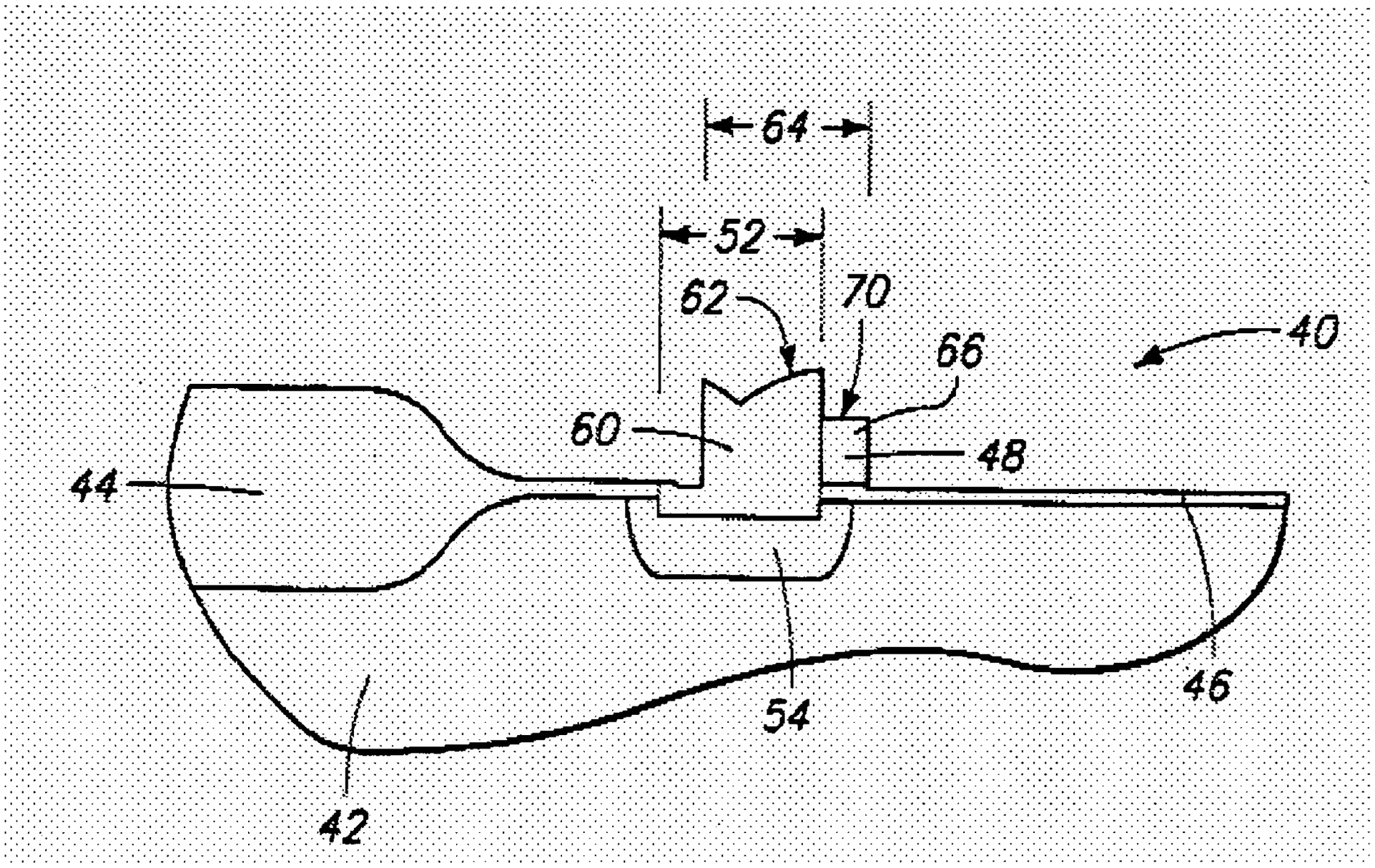
Applicant contends that Tang, U.S. Patent 5,506,172 herein known as Tang is not prior art because Applicants reserve the right to swear behind it at a later date.

Applicant contends that claim 38 is distinguishable from Tang because claim 38 calls for particular relationship between the thickness of the oxide layer and the height of the first poly layer that is shown in the cited Tang patent:

"a first polycrystalline silicon layer overlying the oxide region but not the first substrate region having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region.

Applicants further contend that Tang shows a structure where the first poly layer 48 has its lowest upper surface either lower than or at a height about equal to the highest upper surface of oxide region 44.

In response to Applicants contention that Tang fails to show the claimed limitations as pertaining to claim 38 please see FIG. 9 where Tang teaches the claimed limitation. It appears that Applicants are relying on the features of oxide 44, whereas the Examiner is relying on first polysilicon 48/66 where the lower portion of the polysilicon is above oxide layer 46. Applicants arguments are moot.



Terminal Disclaimer

It fails to disclaim the terminal portion of any patent granted on the subject application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an

international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 38, 39, 40, 41, 42, 43, 44, 45, 47, 53, 54, 55, 56, 58, 60, 61, 62, 64 and 68 are rejected under 35 U.S.C. 102(e) as being anticipated by Tang, U.S. Patent 5,5-6,172.

4. Tang discloses an intermediate in the manufacturing of a semiconductor interconnect as claimed. See **FIGS. 1-13**, where Tang teaches the claimed process.

5. Pertaining to claim 38, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying region of a substrate layer, comprising:

a substrate layer **42** having a first substrate .region and a second substrate region;

an oxide region **44** overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer **48** overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region; and

a second polycrystalline silicon layer **58** overlying the first polycrystalline silicon layer and the first substrate region.

6. Pertaining to claim 39, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer **42** having a first substrate region and a second substrate region;

an oxide region **44** overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer **48** overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer **50** unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer **58** overlying the etch stop layer and the first substrate region.

7. Pertaining to claim 40, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer **42** having a first substrate region and a second substrate region;

an oxide region **44** overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer **48** overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer **50** unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer;

and a second polycrystalline silicon layer **58** overlying the etch stop layer and the first substrate region, the upper surface of the second polycrystalline silicon layer being substantially planar and aligned with the upper surface of the first polycrystalline silicon layer adjacent an interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer such

that the interface has no horizontal component (please note that Applicants drawings are not to scale).

8. Pertaining to claim 41, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer **42** having a first substrate region and a second substrate region;

a field oxide region **44** overlying at least a portion of the second substrate region;

a gate oxide region **46**overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer **48** overlying the field oxide and gate oxide regions but not the first substrate region and having a thickness selected such that the lowest upper surface of the first polycrystalline silicon layer is higher than the highest upper surface of the oxide regions;

an etch stop layer **50** unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

9. Pertaining to claim 42, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer **42** having a first substrate region and a second substrate region;

an oxide region **44** overlying at least a portion of the second substrate region;

a polycrystalline silicon layer **48** overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug **60** overlying the first substrate region and having the upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component; and a photoresist mask of material resistant to polycrystalline silicon etching overlying the polycrystalline silicon plug and an adjacent portion of the first polycrystalline layer surrounding the polycrystalline silicon plug thereby defining an electrical interconnect (The Examiner takes the position that it is well known that photoresist is used as a mask in manufacturing semiconductors).

10. Pertaining to claim 43, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region;

an oxide region overlying at least a portion of the second substrate region; a polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

a polycrystalline silicon plug overlying the first substrate region and having an upper surface thereof aligned with an upper surface of the polycrystalline silicon layer adjacent the second substrate region such that a vertical interface between the polycrystalline silicon layer

and the polycrystalline silicon plug has no horizontal component; and a photoresist mask overlying the polycrystalline silicon plug to define an electrical interconnect.

11. Pertaining to claim 44, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate .region and a second substrate region; at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying the oxide region but not the first substrate region and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

12. Pertaining to claim 45, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region; an oxide region overlying at least a portion of the second substrate region; a polycrystalline silicon plug overlying the first substrate region; and

a polycrystalline silicon layer overlying a portion of the oxide region adjacent the polycrystalline silicon plug, but not the first substrate region, the polycrystalline silicon layer

having a thickness selected such that a lowest upper surface of the polycrystalline silicon layer is higher than a highest upper surface of the oxide region, the polycrystalline silicon layer also having an upper surface thereof in the region adjacent the polycrystalline silicon plug aligned with an upper surface of the polycrystalline silicon plug such that the vertical interface between the polycrystalline silicon layer and the polycrystalline silicon plug has no horizontal component.

13. Pertaining to claim 47, Tang teaches an intermediate in the manufacture of a semiconductor interconnect overlying a region of a substrate layer, comprising:

a substrate layer having a first substrate region and a second substrate region; at least one oxide region overlying at least a portion of the second substrate region;

a first polycrystalline silicon layer overlying a portion of the oxide region adjacent the first substrate region, but not the first substrate region, and having a thickness selected such that a lowest upper surface of the first polycrystalline silicon layer is higher than a highest upper surface of the oxide region;

an etch stop layer unresponsive to a polycrystalline silicon etch overlying the first polycrystalline silicon layer; and

a second polycrystalline silicon layer overlying the first substrate region adjacent the second substrate region such that there is only a vertical interface between the first polycrystalline silicon layer and the second polycrystalline silicon layer.

14. Pertaining to claim 53, Tang teaches the intermediate of claim 38 wherein the first substrate region includes a buried contact region **54**.

15. Pertaining to claim 54, Tang teaches the intermediate of claim 38 wherein a portion of the second polycrystalline layer overlying the first polycrystalline layer is removed to expose the first polycrystalline layer and eliminate a horizontal interface between the first and second polycrystalline silicon layers.

16. Pertaining to claim 55, Tang teaches the intermediate of claim 39 wherein a portion of the second polycrystalline silicon layer overlying the first polycrystalline layer is removed so that a total height of the first polycrystalline silicon layer plus a height of the etch stop layer defines a maximum height of the second polycrystalline silicon layer after removal of the portion of the second polycrystalline silicon layer.

17. Pertaining to claim 56, Tang teaches the intermediate of claim 40 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity (column 3, line 61).

18. Pertaining to claim 58, Tang teaches the intermediate of claim 41 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

19. Pertaining to claim 60, Tang teaches the intermediate of claim 42 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.(the Examiner takes the

position that since a doped polysilicon layer is over a gate oxide layer, it would imply that a field effect transistor is being fabricated).

20. Pertaining to claim 61, Tang teaches the intermediate of claim 43 wherein the polycrystalline silicon plug forms a gate for a field effect transistor.

21. Pertaining to claim 62, Tang teaches the intermediate of claim 44 wherein a photoresist mask is applied over a portion of the first etch stop layer and the second polycrystalline silicon layer.

22. Pertaining to claim 63, Tang teaches the intermediate of claim 62 wherein a titanium layer is deposited to overlie the etch stop layer and the second polycrystalline silicon layer.

23. Pertaining to claim 64, Tang teaches the intermediate of claim 45 wherein the polycrystalline plug and the polycrystalline silicon layer are doped to increase their conductivity.

24. Pertaining to claim 68, Tang teaches the intermediate of claim 47 wherein the first and second polycrystalline silicon layers are doped to increase their conductivity.

Double Patenting

25. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

26. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

27. Claims 38-45, 47-65 and 68-70 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-40 of U.S. Patent No. 6,659,632 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because it is well known that photoresist is used as a mask material in the fabrication of semiconductors.

Conclusion

28. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

29. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on 9:00 AM-5:00 PM.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

32. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC